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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,714	03/18/2004	S. Brandon Keller	200311780-1	6981

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,714	KELLER ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/803,714 filed on 03/18/2004. Claims 1-24 remain pending in the application.

Claim Objections

2. Claim 1 is objected to because following informalities:

Applicant must clarify what is "the circuit" on line 3 (said VLSI circuit/the VLSI circuit?).

3. Claim 9 is objected to because following informalities:

Applicant must clarify what is "the circuit" on line 3 (said VLSI circuit/the VLSI circuit?).

4. Claim 17 is objected to because following informalities:

Applicant must clarify what is "the circuit" on line 4 (said VLSI circuit/the VLSI circuit?).

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (US Patent 5,446,676).

6. As to claims 1, 9 and 17 Huang discloses:

(1) A method of using a software tool to analyze a VLSI circuit, the method comprising (col.4, ll.10-13, Fig. 1):

prior to initiating analysis of the circuit (After completing preprocessing in block 208, simulator 22 constructs static channel connected components in block 210 based on netlist 20, as shown in FIG. 8. A channel connected component ("CCC") is a set of nodes and transistors interconnected through transistor channels - col.11, ll.55-61, Figs. 10, 12), performing a complexity check on the circuit (each newly-created CCC is evaluated for node quantity – col.13, ll.31-32) (col.11, ll.55-65; col.13, ll.20-32);

responsive to the circuit failing the complexity check, aborting analysis of the circuit (All transistors associated with a CCC found to exceed the aforementioned node threshold are classified dynamic by marking "static" flag 138 for each transistor false (see FIG. 9 and Table 2). The "large" CCC structure is then discarded –col.13, ll.32-36); and

responsive to the circuit passing (static CCCs) the complexity check (col.13, ll.48-52):

initiating analysis of the circuit (input events" are initially inserted into the event wheel of the simulator (simulator and analyzer 22 – col.6, ll.36-37) at block 214. These events are simply input vectors created to initiate the simulation – col.14, ll.7-10) (col.14, ll.4-11); and

continuing analysis of the circuit until expiration of a predetermined time

period following the initiating (After event processing for x is complete, the program scans the event wheel for the next pending event in block 222, repeating the process shown in FIG. 8 until the next-pending-event time exceeds total simulation time, at which point, simulator 22 terminates the simulation - col.14, ll.35-40) (col.4, ll.18-19; col.14, ll.10-40);

(9) A computer-implemented tool for analyzing a VLSI circuit, comprising (col.4, ll.10-13, Fig. 1):

means (simulator, Fig.1) for performing a complexity check on the circuit prior to initiating analysis thereof (col.11, ll.55-65; col.13, ll.20-32);

means (simulator, Fig.1) responsive to the circuit failing the complexity check for aborting analysis of the circuit (col.13, ll.32-36);

means responsive (simulator, Fig.1) to the circuit passing the complexity check for initiating analysis of the circuit (col.13, ll.48-52; col.14, ll.4-11); and

means (simulator, Fig.1) for continuing the analysis for a predetermined time period (col.4, ll.18-19; col.14, ll.10-40);

(17) A computer-readable medium operable with a computer to analyze a VLSI circuit, the medium having stored thereon (col.4, ll.10-13; col.6, ll.56-66, Fig. 1):

instructions executable by the computer for performing a complexity check on the circuit prior to initiating analysis thereof (col.11, ll.55-65; col.13, ll.20-32);

instructions executable by the computer responsive to the circuit failing the complexity check for aborting analysis of the circuit (col.13, ll.32-36); and

instructions executable by the computer responsive to the circuit passing the complexity check for initiating analysis of the circuit and continuing analysis the circuit until expiration of a predetermined time period following the initiating (col.4, ll.18-19; col.13, ll.48-52; col.14, ll.4-40).

7. As to claims 2-8, 10-16 and 18-24 Huang recites:

(2), (6), (7), (10), (14), (15), (18), (22), (23) The method/tool/program further comprising halting analysis of the circuit (col.14, ll.33-40);

(3), (11), (19) The method/tool/program further comprising saving data generated during the responsive analysis (col.6, ll.35-41);

(4), (12), (20) The method/tool/program comprises determining whether a number of transistors exceeds a preselected threshold value (col.13, ll.32-37);

(5), (13), (21) The method/tool/program comprises determining whether a number of possible logical paths through the circuit exceeds a preselected threshold value (col.13, ll.20-29);

(5), (13), (21) The method/tool/program comprises initiating a process for verifying reliable operation (Overheated chips and electron migrations in metal lines are but two of the most prominent problems – col.2, ll.16-18) of the circuit (col.2, ll.14-30).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

Thuan Do
THUAN DO
Primary examiner.
5/02/2006